IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Andrew J. Burstein, et al. Art Unit : Unknown
Serial No. : Uassigned Examiner : Unknown
Filed : June 26, 2001
Title : TRANSISTOR PATTERN FOR VOLTAGE REGULATOR

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the title:

Please replace the title "A FLIP-CHIP SWITCHING REGULATOR" with

--TRANSISTOR PATTERN FOR VOLTAGE REGULATOR--

In the specification:

Page 1, line 2, insert the following paragraph:

This application is a continuation of U.S. Patent Application Serial No. 09/498,297, filed February 4, 2000, the entirety of which is incorporated by reference.

In the claims:

Please cancel claims 1-45.

Please add the following new claims:

46. (New) An integrated circuit structure comprising:

a substrate having a first plurality of doped regions and a second plurality of doped regions, the first plurality of doped regions and the second plurality of doped regions being arranged in an alternating pattern; and

a gate region on the substrate separating the first plurality of doped regions and the second plurality of doped regions.

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL631197065US

June 26, 2001
Date of Deposit

47. (New) The integrated circuit structure of claim 46, wherein the first plurality of doped regions and the second plurality of doped regions are arranged in a rectangular array.

48. (New) The integrated circuit structure of claim 46, wherein the gate region is a unitary gate structure separating adjacent doped regions of the first plurality of doped regions and the second plurality of doped regions.

49. (New) The integrated circuit structure of claim 46, wherein the first plurality of doped regions and the second plurality of doped regions are substantially rectangular, and the gate region forms a rectangular grid separating the first plurality of doped regions and the second plurality of doped regions.

50. (New) The integrated circuit structure of claim 46, wherein the first plurality of doped regions are source regions of a distributed transistor array and the second plurality of doped regions are drain regions of the distributed transistor array.

51. (New) The integrated circuit structure of claim 50, wherein the distributed transistor array operates as a switch in a switching regulator circuit.

52. (New) The integrated circuit structure of claim 50, wherein the distributed transistor array is a PMOS transistor.

53. (New) The integrated circuit structure of claim 50, wherein the distributed transistor array is an NMOS transistor.

54. (New) A voltage regulator having an input terminal and an output terminal, comprising:

a printed circuit board;

a first flip-chip type integrated circuit chip mounted on the printed circuit board, the first integrated circuit chip including a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal, wherein the power switch includes

a chip substrate having a first plurality of doped regions and a second plurality of doped regions, the first plurality of doped regions and the second plurality of doped regions being arranged in an alternating pattern, the first plurality of doped regions coupled to the input terminal, the second plurality of doped regions coupled to the output terminal, and

a gate region on the chip substrate separating the first plurality of doped regions and the second plurality of doped regions;

a filter disposed to provide a substantially DC voltage at the output terminal; and

a control circuit connected to the gate region to control the power switch to maintain the DC voltage substantially constant.

55. (New) The voltage regulator of claim 54, wherein the first plurality of doped regions and the second plurality of doped regions are arranged in a rectangular array.

56. (New) The voltage regulator of claim 54, wherein the gate region is a unitary gate structure separating adjacent doped regions of the first plurality of doped regions and the second plurality of doped regions.

57. (New) The voltage regulator of claim 54, wherein the first plurality of doped regions and the second plurality of doped regions are substantially rectangular, and the gate region forms a rectangular grid separating the first plurality of doped regions and the second plurality of doped regions.

58. (New) The voltage regulator of claim 54, wherein the first plurality of doped regions are source regions of a distributed transistor array and the second plurality of doped regions are drain regions of the distributed transistor array.

59. (New) The voltage regulator of claim 58, wherein the distributed transistor array is a PMOS transistor.

60. (New) The voltage regulator of claim 58, wherein the distributed transistor array is an NMOS transistor.

61. (New) The voltage regulator of claim 54, wherein the first power switch and filter form a buck-converter topology.

62. (New) The voltage regulator of claim 54, wherein the first power switch intermittently couples an intermediate terminal to the input terminal.

63. (New) The voltage regulator of claim 62, wherein the first flip-chip type integrated circuit chip has a second power switch fabricated therein to alternately couple and decouple the intermediate terminal to ground.

64. (New) The voltage regulator of claim 63, wherein the filter is electrically coupled between the output terminal and the intermediate terminal.

65. (New) The voltage regulator of claim 63, wherein the first power switch includes a distributed array of PMOS transistors and the second power switch includes a distributed array of NMOS transistors.

66. (New) The voltage regulator of claim 62, further comprising a rectifier connecting the intermediate terminal to ground.

67. (New) An integrated circuit chip with a power switch for a voltage regulator fabricated thereon, comprising:

a substrate having a first plurality of doped regions and a second plurality of doped regions, the first plurality of doped regions and the second plurality of doped regions being arranged in a first alternating pattern;

a gate region on the substrate separating the first plurality of doped regions and the second plurality of doped regions; and

an array of metalized pads fabricated on a surface of the substrate, the array including a first plurality of pads and a second plurality of pads, the first and second pluralities of pads being arranged in a second alternating pattern;

wherein the first plurality of pads are electrically connected to the first plurality of doped regions and the second plurality of pads are electrically connected to the second plurality of

doped regions, and wherein the first plurality of pads are connected to a first terminal of the voltage regulator and the second plurality of pads are connected to a second terminal in the voltage regulator.

68. (New) The chip of claim 67, wherein the first alternating pattern is a rectangular array.

69. (New) The chip of claim 67, wherein the gate region is a unitary gate structure separating adjacent doped regions of the first plurality of doped regions and the second plurality of doped regions.

70. (New) The chip of claim 67, wherein the first plurality of doped regions and the second plurality of doped regions are substantially rectangular, and the gate region forms a rectangular grid separating the first plurality of doped regions and the second plurality of doped regions.

71. (New) The chip of claim 67, wherein the first plurality of doped regions are source regions of a distributed transistor array and the second plurality of doped regions are drain regions of the distributed transistor array.

72. (New) The chip of claim 71, wherein the distributed transistor array operates as a switch in a switching regulator circuit.

73. (New) The chip of claim 67, wherein the second alternating pattern is a first set of alternating stripes.

74. (New) The chip of claim 67, wherein the second alternating pattern is a checkerboard pattern.

75. (New) The chip of claim 67, wherein the first and second pluralities of doped regions are p+ regions formed in an n-type well or substrate.

76. (New) The chip of claim 75, wherein the first terminal is an input terminal and the second terminal is an intermediate terminal.

77. (New) The chip of claim 67, wherein the first and second pluralities of doped regions are n+ regions formed in a p-type well or substrate.

78. (New) The chip of claim 77, wherein the first terminal is a ground terminal and the second terminal is an intermediate terminal.

REMARKS

Applicant submits that the claims are in condition for examination.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 6/26/01

David Goren

David J. Goren
Reg. No. 34,609

Fish & Richardson P.C.
2200 Sand Hill Road, Suite 100
Menlo Park, CA 94025
Telephone: (650) 322-5070
Facsimile: (650) 854-0875

50051566.doc